PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number
20880-05093

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on _____

Signature _____

Typed or printed name _____

Application Number	Filed
09/748,098	December 21, 2000
First Named Inventor	
Nicholas J. Kelsey	
Art Unit	**Examiner**
2183	David J. Huisman

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.

☒ attorney or agent of record.
Registration number 57,219

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/Brian G. Brannon/
Signature

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August 23, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of one form is submitted.

REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW IN U.S. PATENT APPLICATION NO. 09/748,098 FILED ON DECEMBER 21, 2000

Pre-appeal brief review is appropriate in this application because the rejections in the Final Office Action dated May 23, 2007 contain clear deficiencies. Applicants request that the rejections of claims 1-55 be withdrawn. As set forth below, these rejections are deficient because the cited references fail to include any teaching or suggestion of at least one essential claim element.

REJECTION OF CLAIMS 2-18 AND 19-28 UNDER 35 USC 112

Claims 2-18 and 19-28 have been rejected under 35 U.S.C. 112, ¶1 and ¶2 as allegedly failing to comply with the enablement requirement and allegedly failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Examiner states that "As is known, an instruction cycle (or clock cycle) is a period of time in which a clock oscillates from low to high." *See* Final Office Action, paragraph 6, page 3. Contrary to Examiner's statement, as known in the art, an instruction cycle is not the same as a clock cycle. It is well known in the art that an instruction cycle is the execution of an instruction by a processor, including fetching the instruction from memory, decoding and executing the instruction. *See, e.g.,* Jack Ganssle and Michael Barr, *Embedded Systems Dictionary,* CMP Books, 2003, p. 138 ("instruction cycle: n. The time it takes to fetch and execute a single opcode."). Hence, "between consecutive instruction cycles," describes the interval between fetching a first instruction and fetching a second instruction. It is well known in the art that to fetch and execute an instruction multiple clock cycles of a processor clock may be required.

Examiner relied on a Wikipedia reference to show "the concept behind a clock cycle, i.e., an instruction cycle, and how there is no between cycles." *See* Final Office Action, paragraph 77, page 32. Applicants object to Examiner's reliance on such an unreliable source as objective

evidence of the state of the art at the time the applicants filed their application. However, even a search of Wikipedia for "instruction cycle," as claimed, yields:

> The instruction cycle (also called fetch-and-execute cycle, fetch-decode-execute cycle (FDX) can refer to either time period during which one instruction is fetched from memory and executed when a computer receives a machine language instruction…

(http://en.wikipedia.org/wiki/Instruction_cycle). Hence, an "instruction cycle" refers to the actions taken by a processor to execute an instruction, not the "period of time in which a clock executes from low to high" as the Examiner incorrectly asserts. The specification variously discloses thread switching between "instruction cycles" or "machine instructions," rather than switching between "clock cycles" at, for example, page 7, lines 16-26 and page 17, lines 1-24.

As explained above, "instruction cycle" describes actions taken by a processor to execute an instruction, so the system is **not** operating during an instruction cycle at any point in time as the Examiner asserts, but only when an instruction is being executed. Thus, Applicants respectfully submit that the specification contains "a written description of the invention…in such full, clear, concise and exact terms as to enable any person skilled in the art to which it pertains…to make and use the same." See 35 U.S.C. §112 (emphasis added).

REJECTION OF CLAIMS 1, 29-33, 42, 43 and 45-47 UNDER 35 USC 102

Claims 1, 29-33, 42, 43 and 45-47 were rejected under 35 USC §102(e) as allegedly being anticipated by U.S. Patent No. 6,076,157 to Borkenhagen et al. ("Borkenhagen"). This rejection is respectfully traversed.

Claim 1 recites "causing thread-switching at a fixed time according to a predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles." This predetermined fixed schedule beneficially provides a predict-

able execution time for threads, and allows execution of each thread in a sequence specified by the predetermined fixed schedule.

In contrast, Borkenhagen discloses a multithreaded processor including "a time-out register which forces a thread switch when execution of the active thread in the multi-threaded processor exceeds a programmable period of time." *See* Borkenhagen, Abstract. Hence, the time-out register imposes an upper-limit on thread execution and forces a thread switch when the upper-limit is reached. *See* Borkenhagen, col. 5, lines 45-55. However, this merely switches processing from a first thread to any other thread after the time-out value is reached and does not switch to a second thread identified by a "predetermined fixed schedule" as claimed.

By failing to provide any reference disclosing "thread-switching at a fixed time according to a predetermined fixed schedule, said schedule specifying that the first thread should be allocated processing time every first number of cycles and that the second thread should be allocated processing time every second number of cycles," the Examiner has failed to establish *prima facie* anticipation and therefore these rejections are improper.

REJECTION OF CLAIMS 1, 29-33, 42, 43 and 45-47 UNDER 35 USC 102

Claims 2-3, 13, 16-17 and 19-24 were rejected under 35 USC §103(a) as allegedly being unpatentable in view of U.S. Patent No. 6,542,991 to Joy ("Joy") and U.S. Patent No. 6,493,741 to Emer et al ("Emer"). This rejection is respectfully traversed.

Claim 17 recites, "said thread selection hardware in the pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles." Claim 19 similarly recites "switching the pipelined processor from executing the first program thread to executing the second program thread between the end of an execution cycle and before the beginning of a next consecutive execution cycle." Switching threads between consecutive instruction cycles beneficially allows switching between different program contexts without in-

curring a time penalty. Switching from one thread to another between the end of an execution cycle before the beginning of a next consecutive instruction cycle beneficially allows thread switching without loss of execution cycles.

Joy does not disclose "said thread selection hardware in the pipelined processor switches from said first thread state to said second thread state between consecutive instruction cycles in response to the hardware thread schedule identifying which of said program threads said pipelined processor executes." Rather, Joy discloses "oblivious thread switching" in which a processor switches threads every N cycles. Joy, col. 17, lines 1-4. Examiner states that "Since there is no disclosed restriction as to what value N might be, a thread switch may occur every cycle (N=1)." *See* Final Office Action, paragraph 28, page 14. However, not only is that not disclosed in the reference, but switching threads every cycle merely changes the executed thread once the next instruction cycle begins, rather than "between the end of an execution cycle and before the beginning of a next consecutive execution cycle" as claimed. Hence, threads are not switched until after the next instruction cycle begins, using part of the instruction cycle to switch, rather than execute, threads.

The deficiencies in Joy are not rectified by Emer, which describes a conventional multi-threaded architecture:

> On any given cycle, a processor executes instructions from just one of the threads. *On the next cycle, it switches to a different thread context* and executes instructions from the new thread. (emphasis added)

Emer, col. 1, lines 54-58. Like Joy, Emer discloses switching between threads after a new cycle begins, not switching "between consecutive instruction cycles" as claimed.

By failing to provide any references that disclose or suggest "switching the pipelined processor from executing the first program thread to executing the second program thread between the end of an execution cycle and before the beginning of a next consecutive execution

cycle," or switching "from said first thread state to said second thread state between consecutive instruction cycles," as claimed, the Examiner has failed to establish a *prima facie* case of obviousness and therefore these rejections are improper.

REJECTION OF CLAIMS 5-12, 14, 15, 18, 25-28, UNDER 35 USC 103

Claims 5-12, 14, 15, 18, and 25-28 were rejected under 35 USC §103(a) as allegedly being unpatentable over Joy and Emer in combination with U.S. Patent No. 6,085,215 to Ramakrishnan et al. ("Ramakrishnan"), Borkenhagen and U.S. Patent No. 6,314,511 to Levy et al. ("Levy"). These rejections are traversed because, as discussed above, none of the cited references disclose or suggest "switching the pipelined processor from executing the first program thread to executing the second program thread between the end of an execution cycle and before the beginning of a next consecutive execution cycle," or switching "from said first thread state to said second thread state between consecutive instruction cycles," as claimed.

REJECTION OF CLAIMS 34-41, 44 AND 48-55, UNDER 35 USC 103

Claims 34-41, 44 and 48-55 were rejected under 35 USC §103(a) as allegedly being unpatentable over Borkenhagen in combination with Ramakrishnan and Levy. These rejections are traversed because, as discussed above, none of the cited references disclose or suggest "causing thread-switching at a fixed time according to a predetermined fixed schedule," as claimed.

Respectfully submitted,

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